

Fig. 1 PRIOR ART

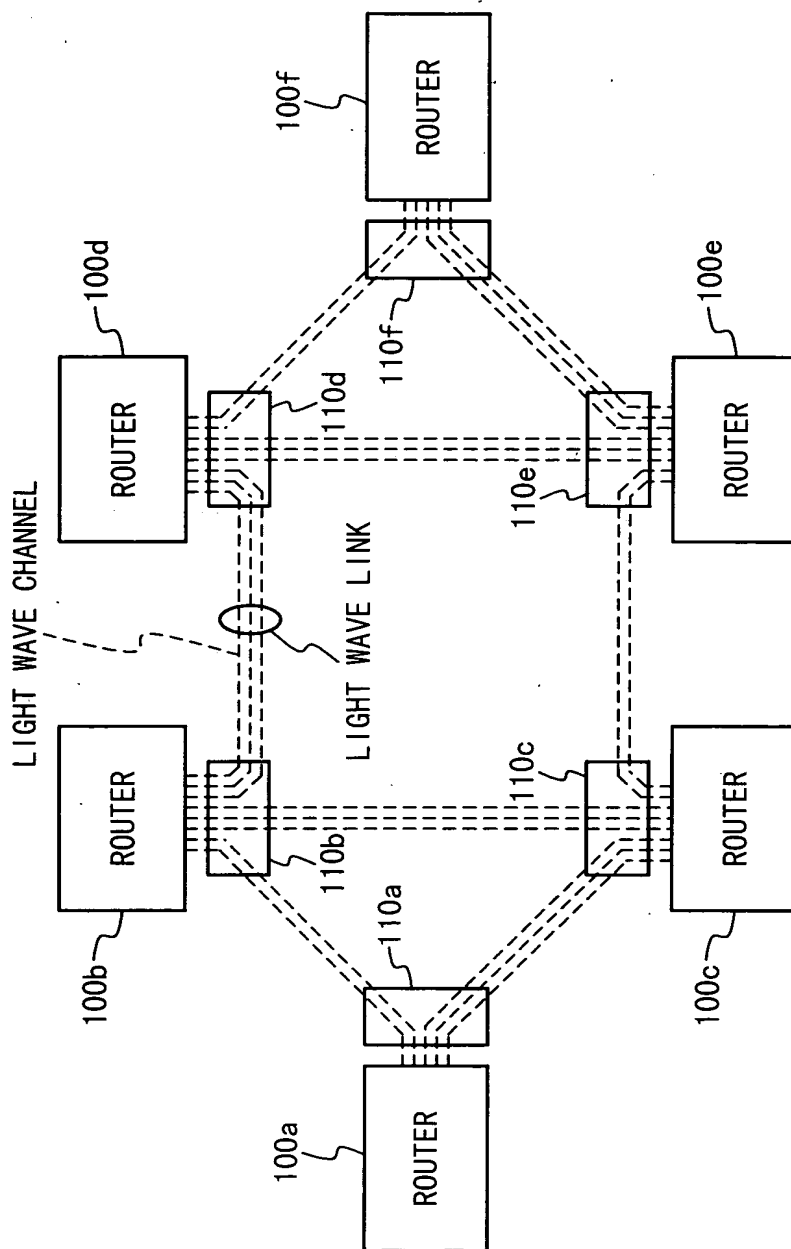


Fig. 2 PRIOR ART

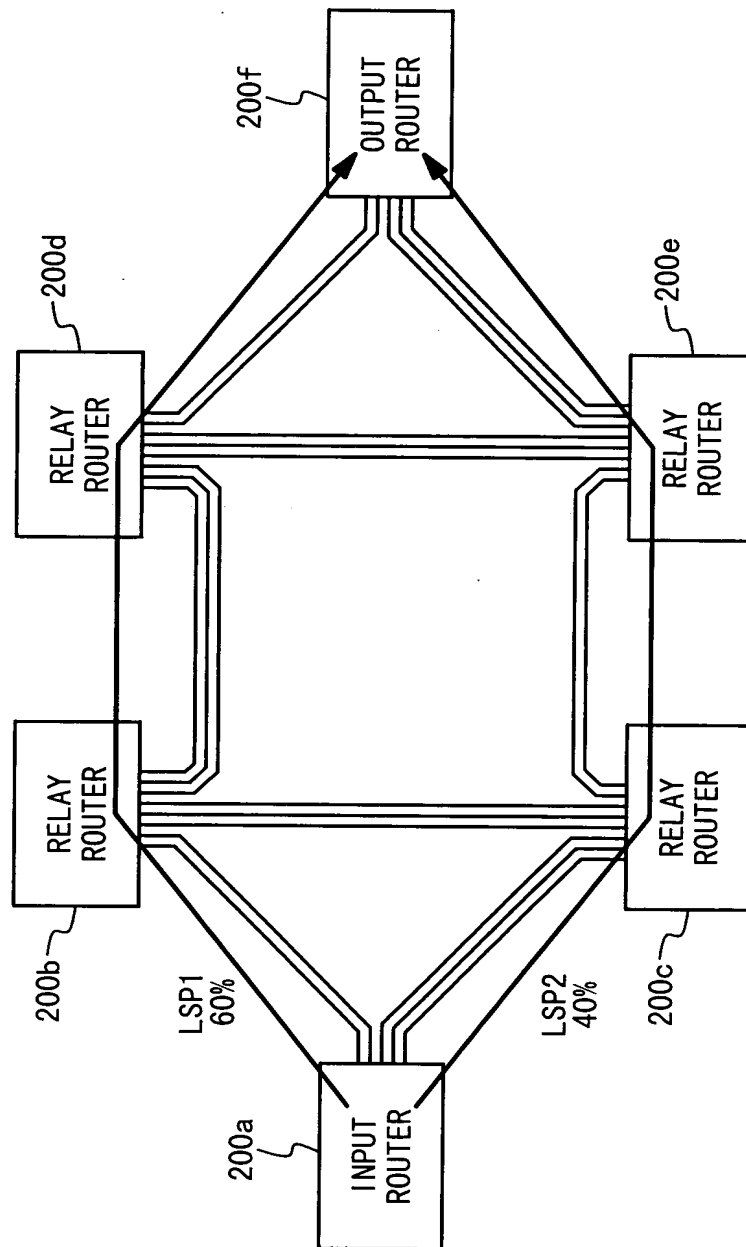


Fig. 3 PRIOR ART

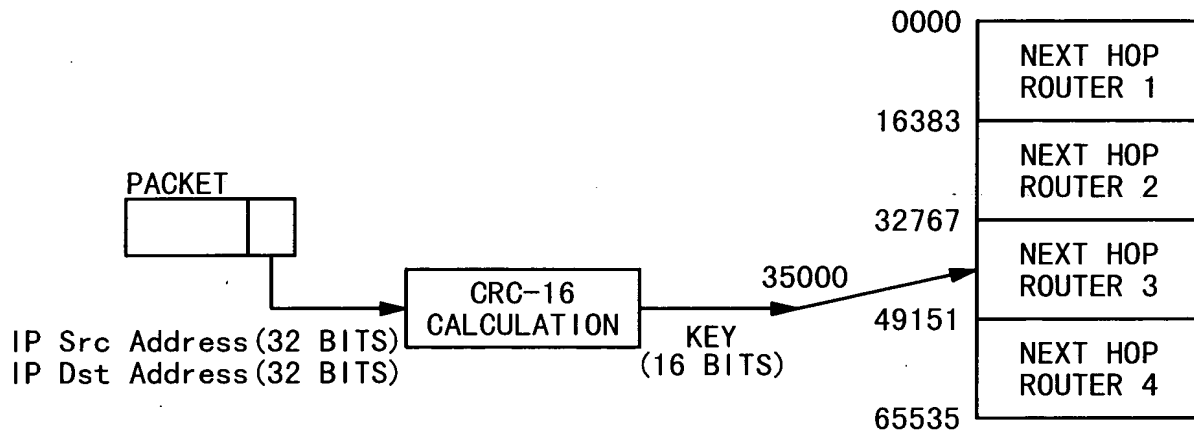


Fig. 4A PRIOR ART

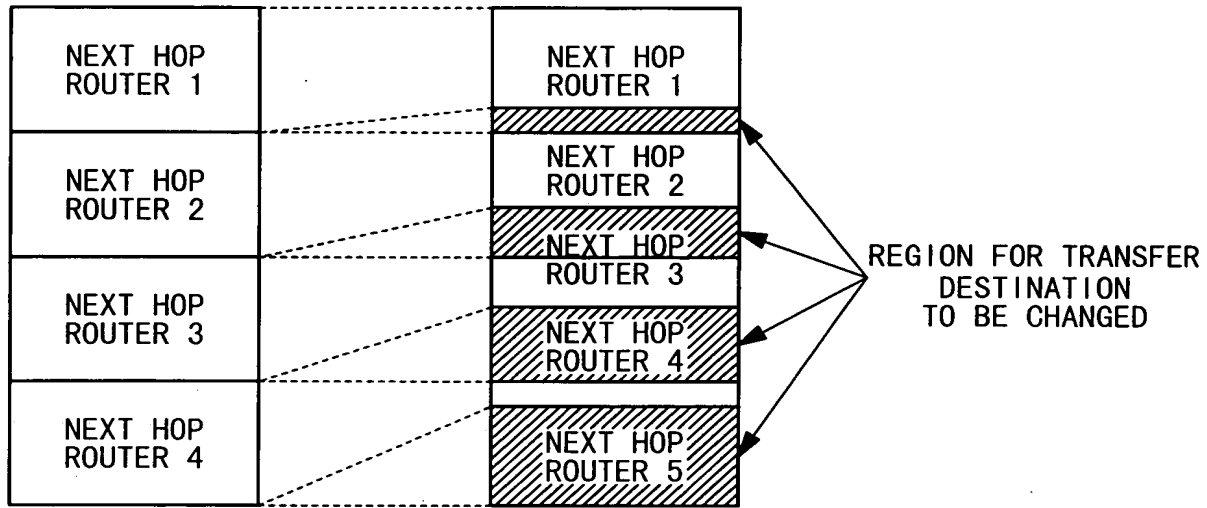


Fig. 4B PRIOR ART

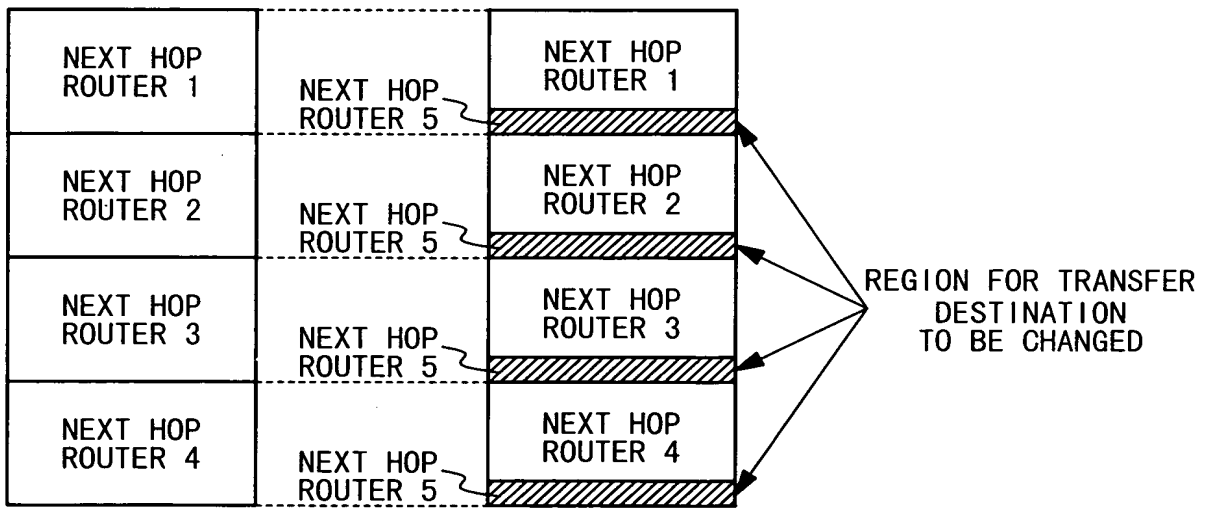


Fig. 5

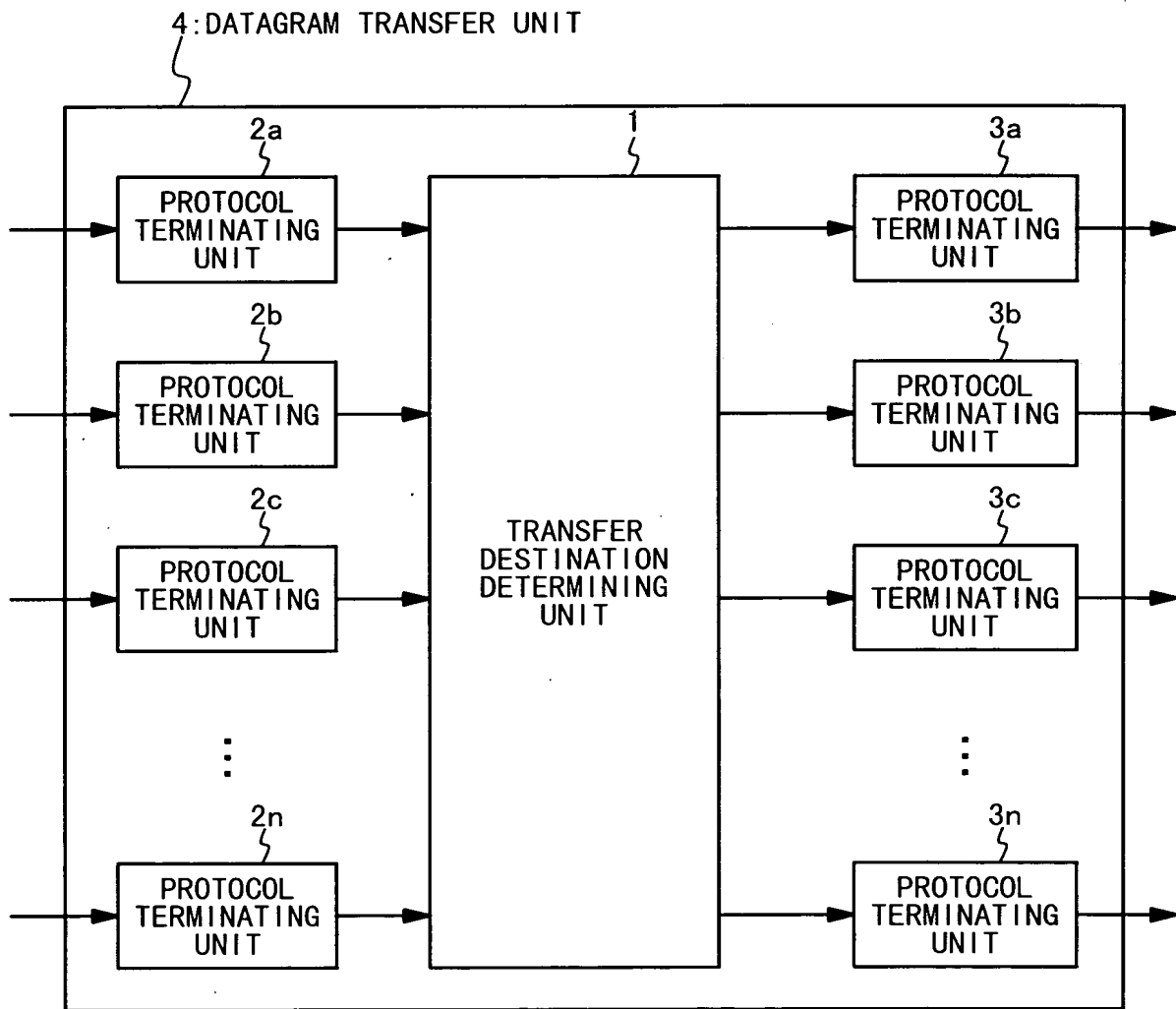


Fig. 6

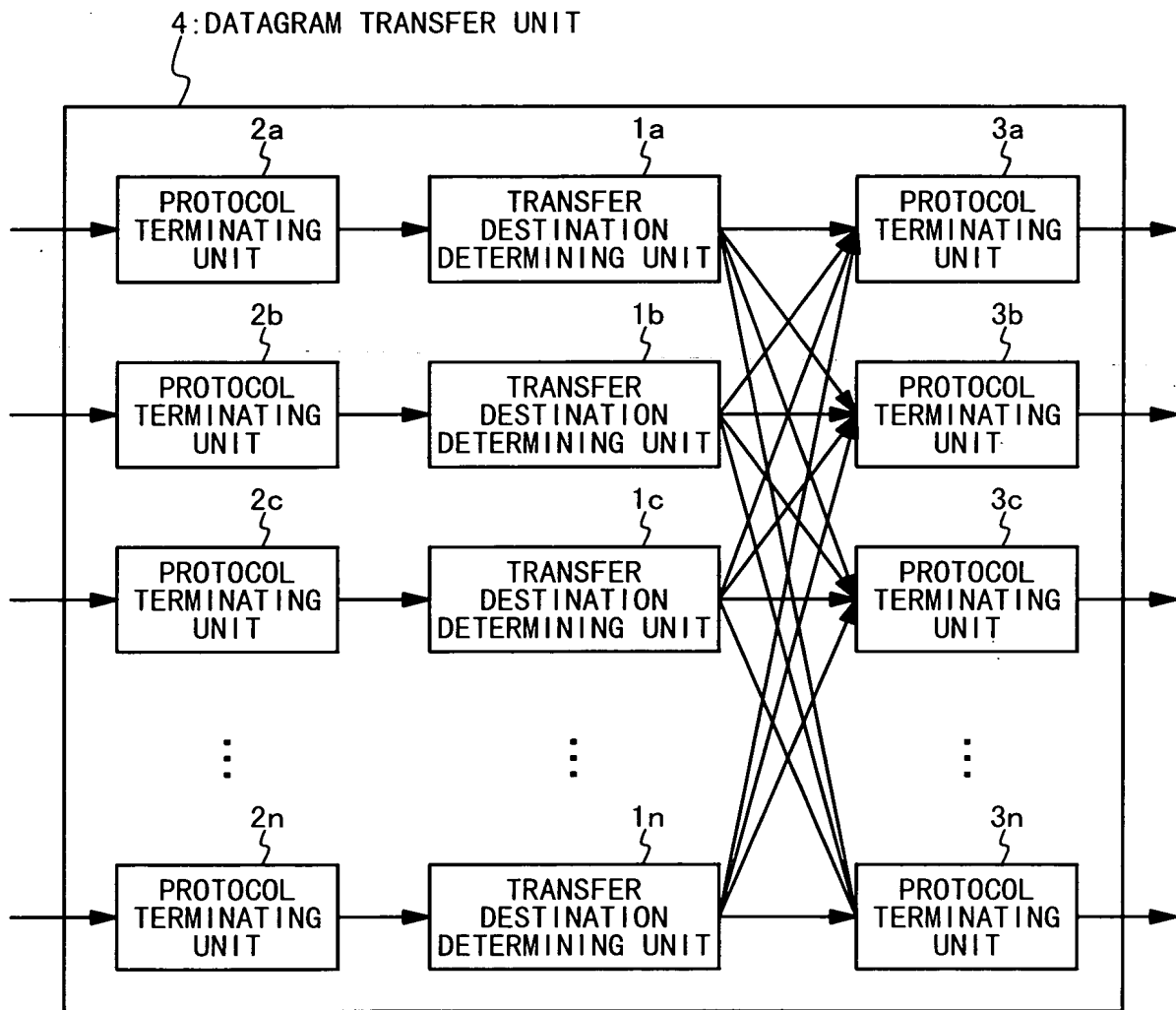


Fig. 7

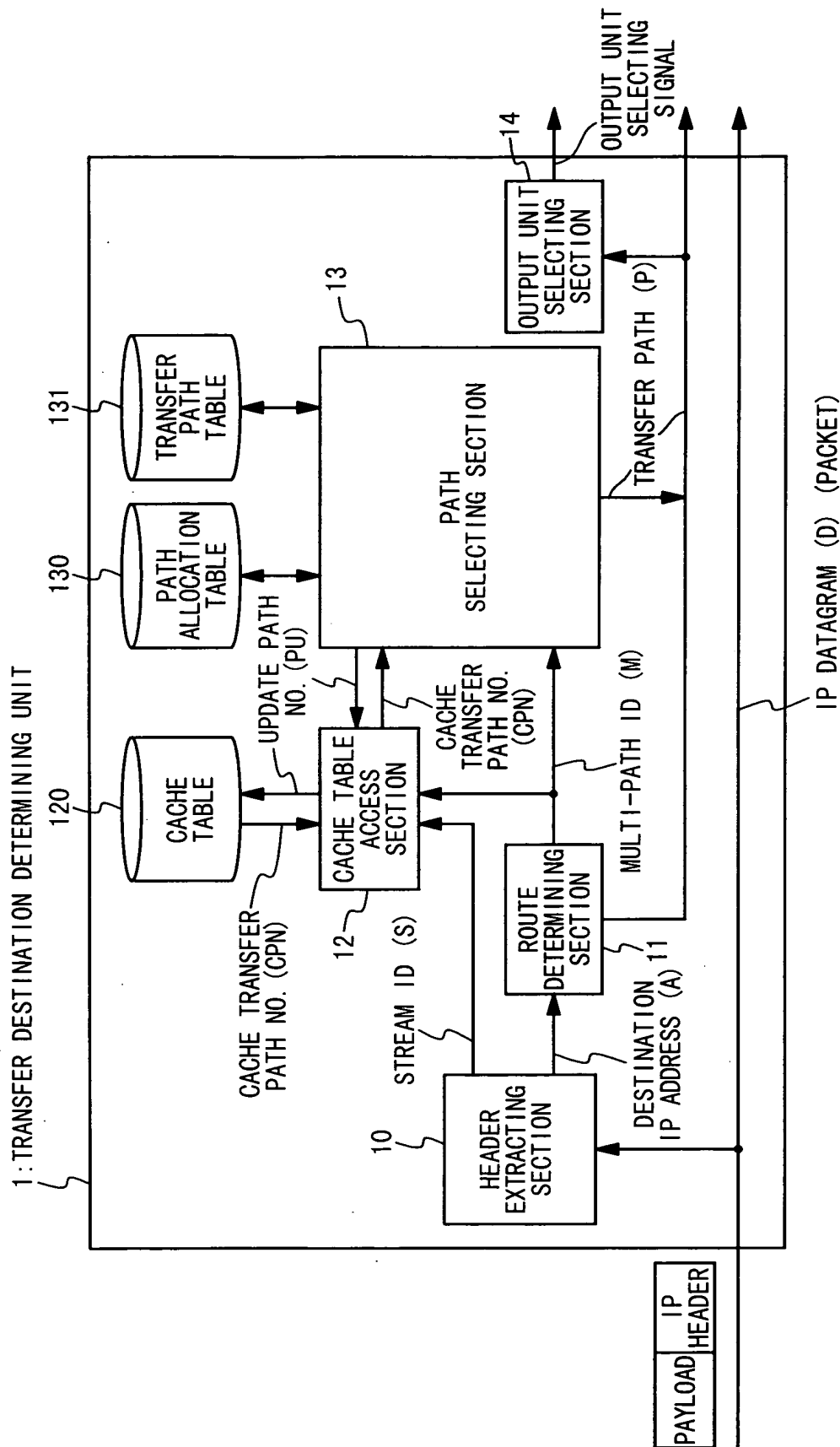


Fig. 8

120: CACHE TABLE

ADDRESS SECTION		DATA SECTION
MULTI-PATH ID (M)	STREAM ID (S)	CACHE TRANSFER PATH NO. (CPN)
0	000	1
	001	2
	002	0
	003	NON REGISTERED
	004	NON REGISTERED
	005	0
	⋮	⋮
	FFF	3
1	000	1
	001	NON REGISTERED
	002	2

Fig. 9

130: PATH ALLOCATION TABLE

ADDRESS SECTION	DATA SECTION			
MULTI-PATH ID (M)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	00000000	00000000	1	1
1	11110000	11110000	2	2
2	11110010	11110010	3	0
3	11111001	11111001	3	0

⋮

CORRESPONDING TO PN = 7

⋮

CORRESPONDING TO PN = 0

Fig. 10

131: TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION			
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)	TRANSFER PATH (P)
0	0	600	3 × 256	3	PATH 0-0
	1	650	3 × 256	3	PATH 0-1
	2	1000	5 × 256	5	PATH 0-2
	3	1200	5 × 256	5	PATH 0-3
	4	0	0	0	NONE
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE
1	0	1500	6 × 256	1	PATH 1-0
	1				
	2				
	3				

⋮

⋮

FIG. 10

Fig. 11

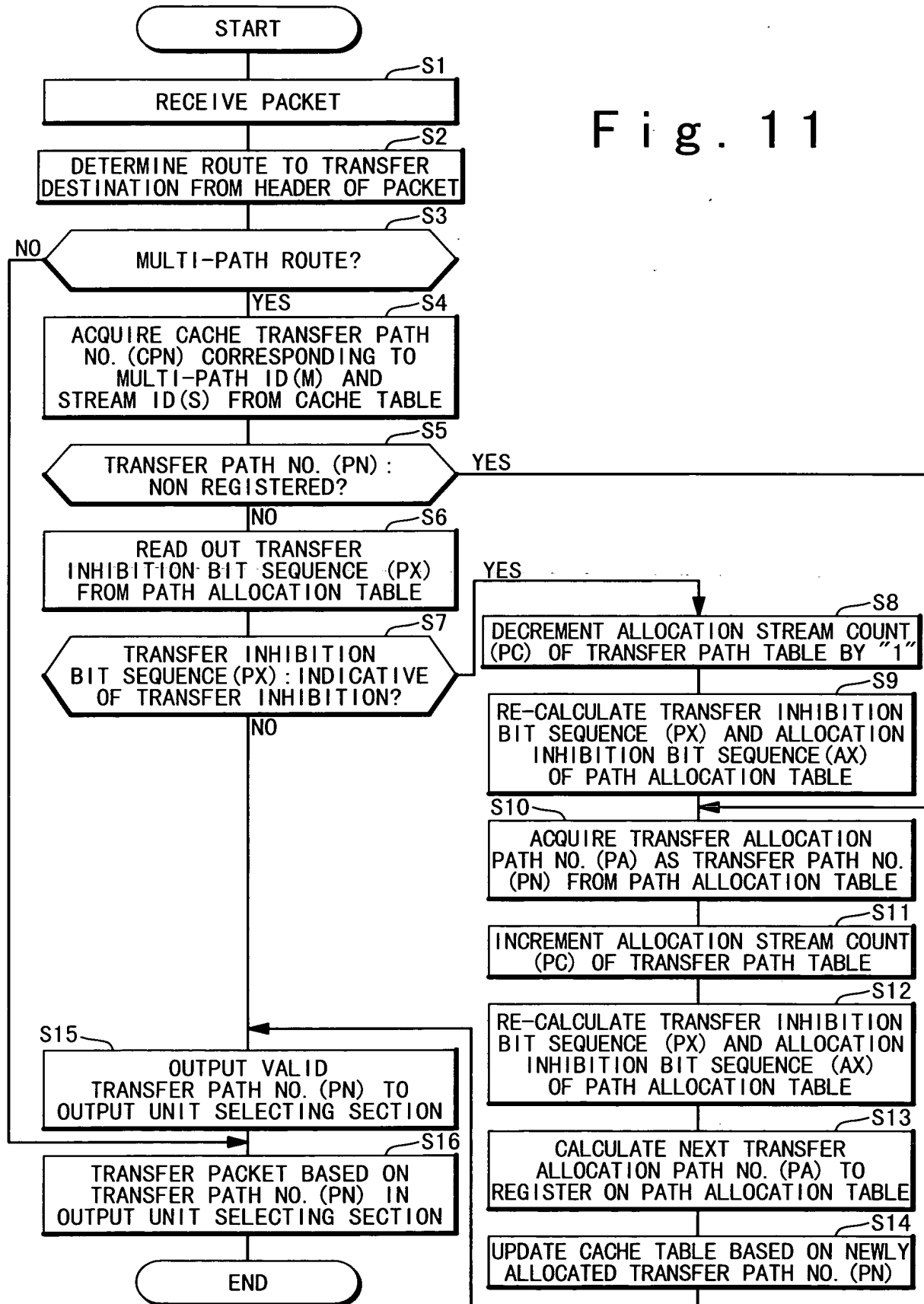


FIG. 11

Fig. 12

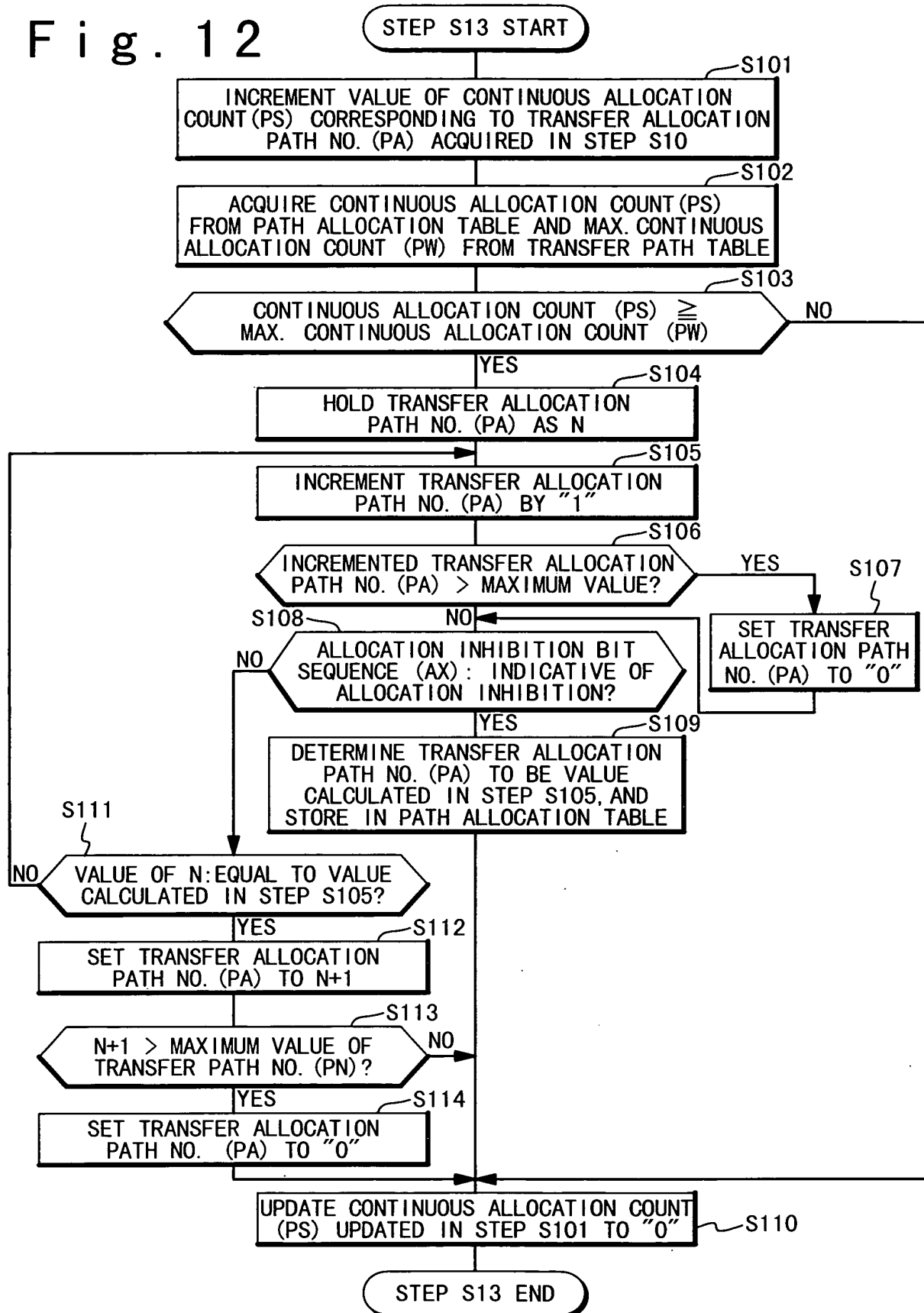


FIG. 12

Fig. 13

130: PATH ALLOCATION TABLE

ADDRESS SECTION	DATA SECTION			
MULTI-PATH ID (M)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	11100000	11100000	0	0

Fig. 14

131: TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION			
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)	TRANSFER PATH (P)
0	0	0	2×256	2	PATH 0-0
	1	0	3×256	3	PATH 0-1
	2	0	5×256	5	PATH 0-2
	3	0	5×256	5	PATH 0-3
	4	0	1×256	1	PATH 0-4
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE

Fig. 15

130: PATH ALLOCATION TABLE

ADDRESS SECTION	DATA SECTION			
MULTI-PATH ID (M)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	11100000	11111111	-	-

Fig. 16

131: TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION			
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)	TRANSFER PATH (P)
0	0	2×256	2×256	0	PATH 0-0
	1	3×256	3×256	0	PATH 0-1
	2	5×256	5×256	0	PATH 0-2
	3	5×256	5×256	0	PATH 0-3
	4	1×256	1×256	0	PATH 0-4
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE

Fig. 17

130: PATH ALLOCATION TABLE

ADDRESS SECTION		DATA SECTION		
MULTI-PATH ID (M)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	11001100	11001110	0	0

Fig. 18

131: TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION			
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)	TRANSFER PATH (P)
0	0	2×256	4×256	2	PATH 0-0
	1	3×256	3×256	0	PATH 0-1
	2	5×256	3×256	0	PATH 0-2
	3	5×256	0	0	(PATH 0-3)
	4	1×256	4×256	3	PATH 0-4
	5	0	1×256	1	PATH 0-5
	6	0	0	0	NONE
	7	0	0	0	NONE

Fig. 19

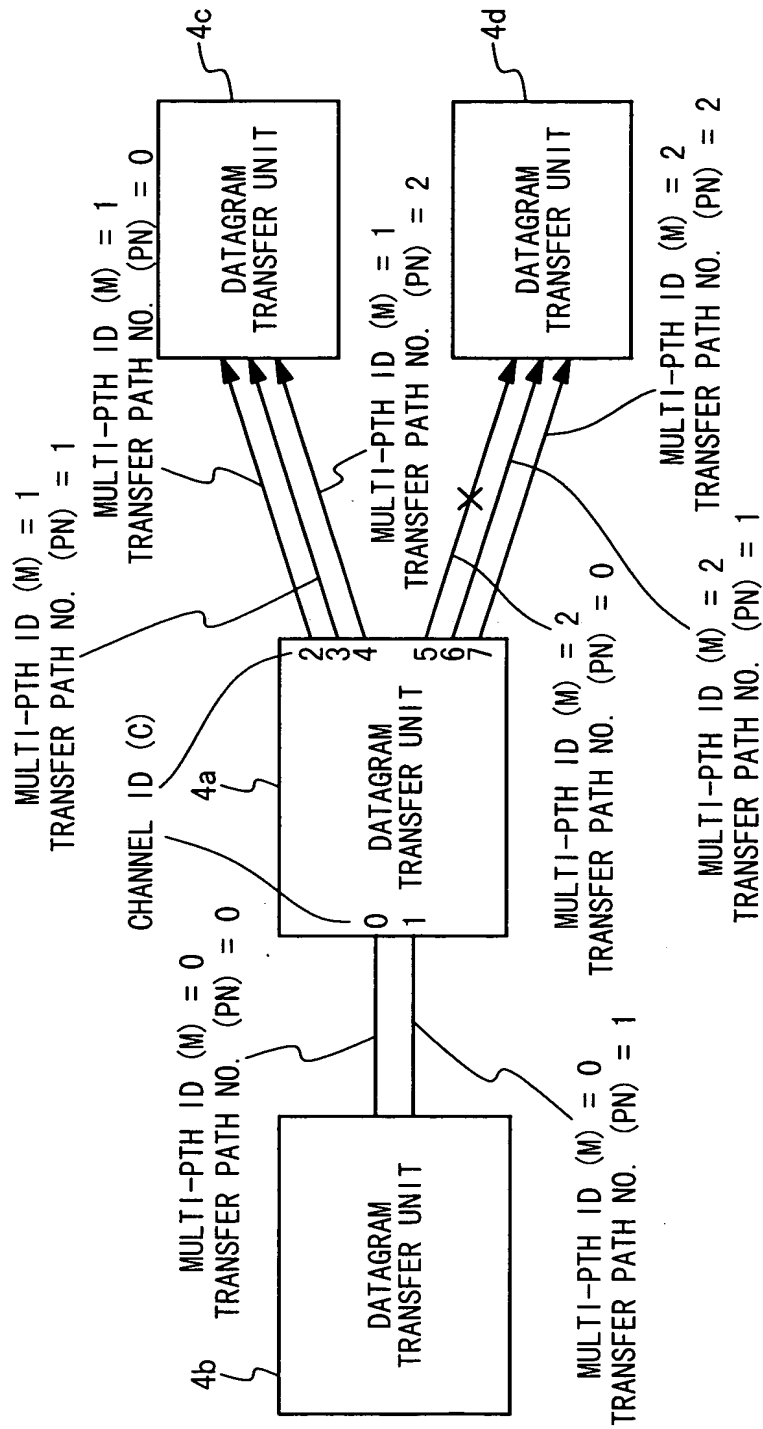


Fig. 20

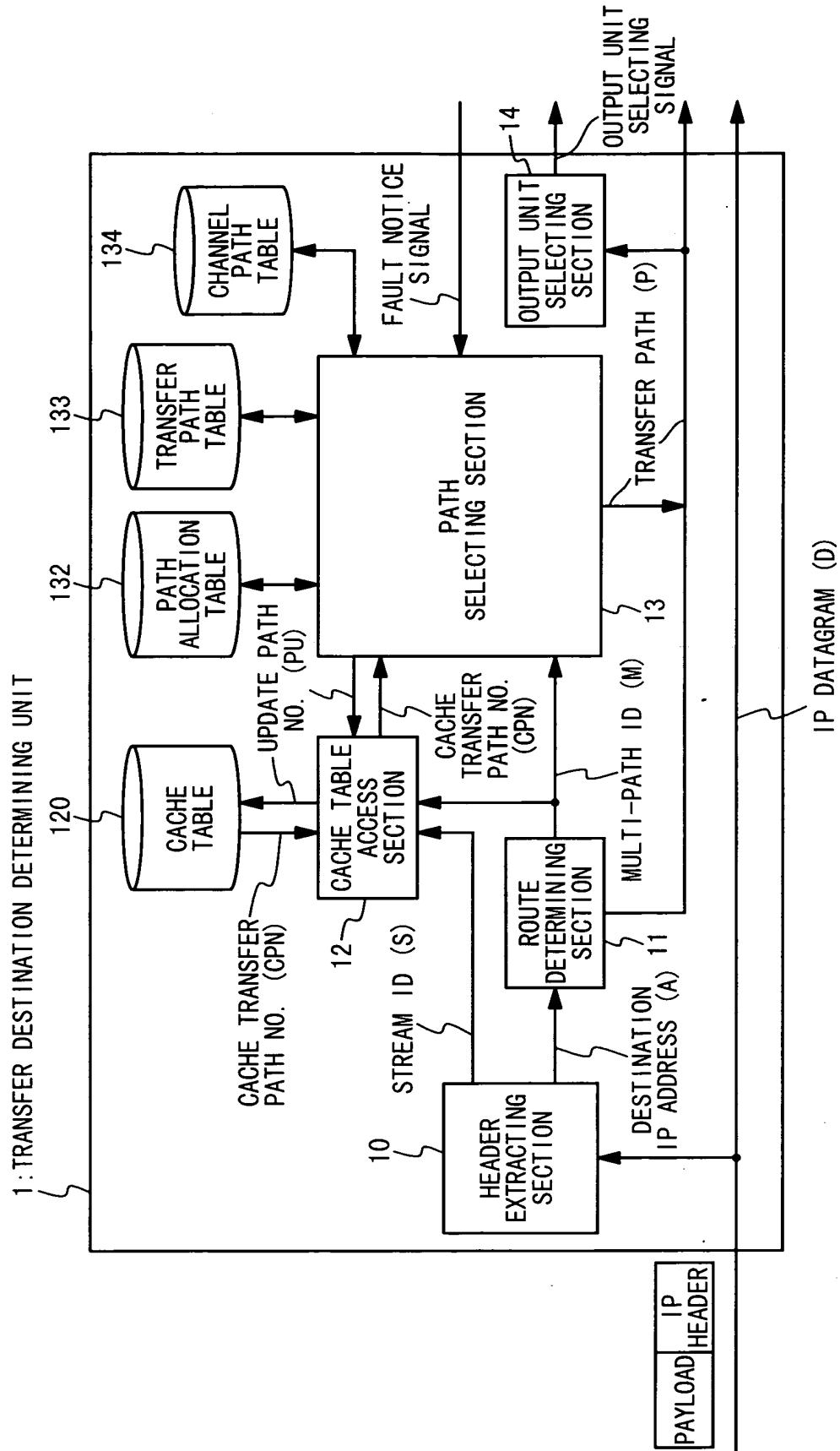


Fig. 21

134: CHANNEL PATH TABLE

ADDRESS SECTION	DATA SECTION	
CHANNEL ID (C)	MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)
0	0	0
1	0	1
2	1	0
3	1	1
4	1	2
5	2	0
6	2	1
7	2	2

Fig. 22

132: PATH ALLOCATION TABLE

ADDRESS SECTION		DATA SECTION					
MULTI-PATH ID (M)	OPERATION MODE (AM)	TRANSFER PATH STATUS BIT SEQUENCE (PD)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)	
0	NORMAL	11111100	11111100	11111111	0	0	
1	NORMAL	11111000	11111000	11111111	0	0	
2	NORMAL	11111000	11111000	11111111	0	0	

Fig. 23

133: TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION			
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)	TRANSFER PATH (P)
0	0	2048	2048	1	PATH 0-0
	1	2048	2048	1	PATH 0-1
	2	0	0	0	NONE
	3	0	0	0	NONE
	4	0	0	0	NONE
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE
1	0	1365	1365	1	PATH 1-0
	1	1365	1365	1	PATH 1-1
	2	1366	1366	1	PATH 1-2
	3	0	0	0	NONE
	4	0	0	0	NONE
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE
2	0	1365	1365	1	PATH 2-0
	1	1365	1365	1	PATH 2-1
	2	1366	1366	1	PATH 2-2
	3	0	0	0	NONE
	4	0	0	0	NONE
	5	0	0	0	NONE
	6	0	0	0	NONE
	7	0	0	0	NONE

FIG. 23

Fig. 24

132: PATH ALLOCATION TABLE

ADDRESS SECTION		DATA SECTION					
MULTI-PATH ID (M)	OPERATION MODE (AM)	TRANSFER PATH STATUS BIT SEQUENCE (PD)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)	
0	NORMAL	11111100	11111100	11111111	0	0	
1	NORMAL	11111000	11111000	11111111	0	0	
2	FAULT STATE	11111001	11111000	11111111	0	0	

Fig. 25

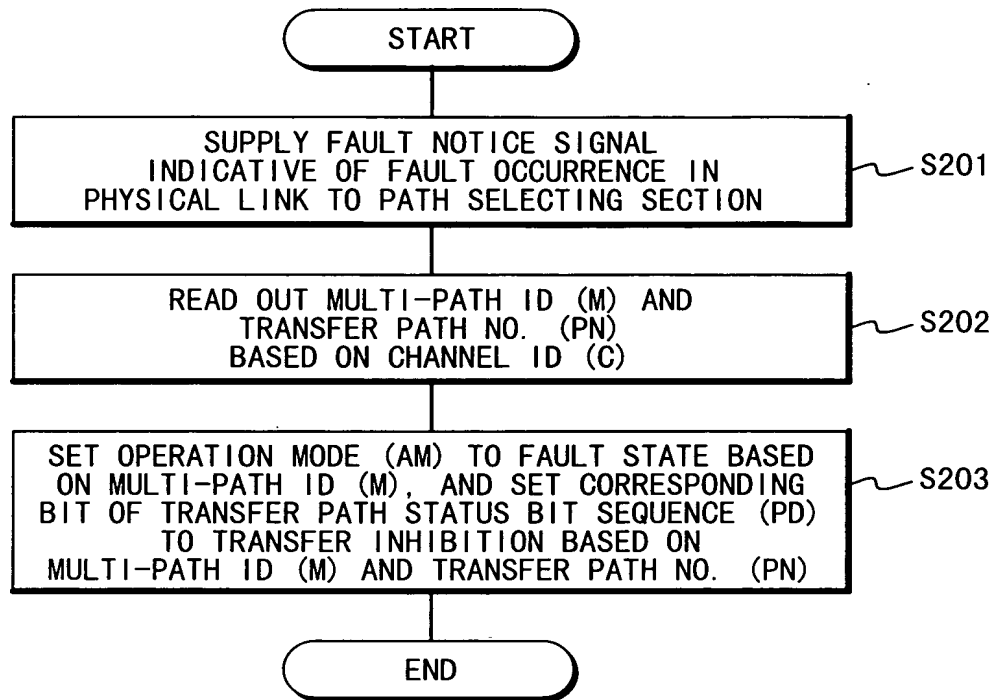


Fig. 26

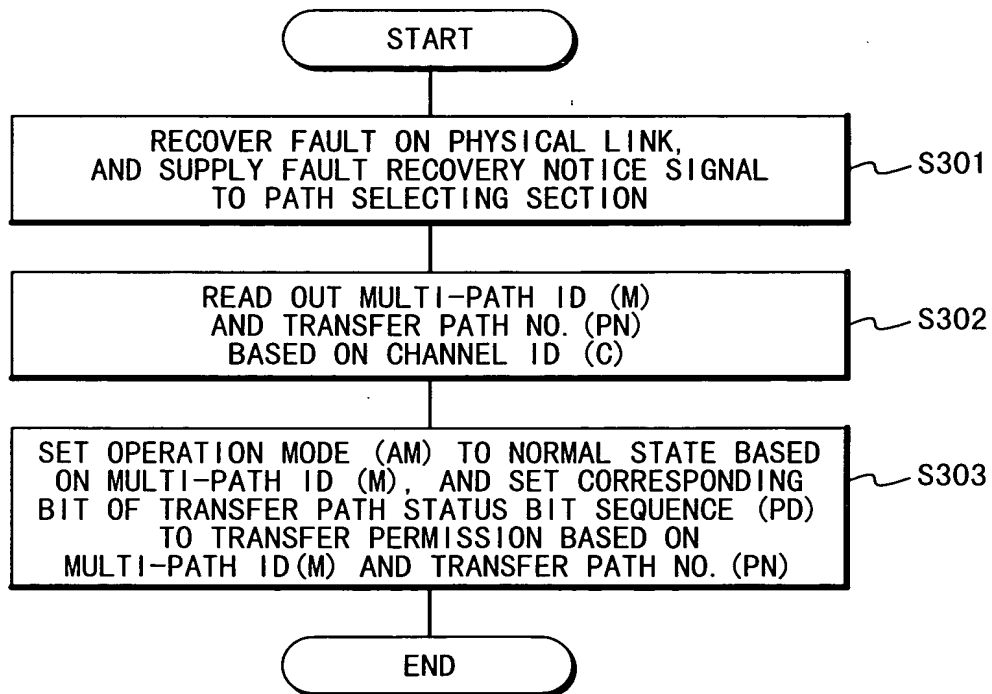


Fig. 27A

Fig. 27

Fig. 27A

Fig. 27B

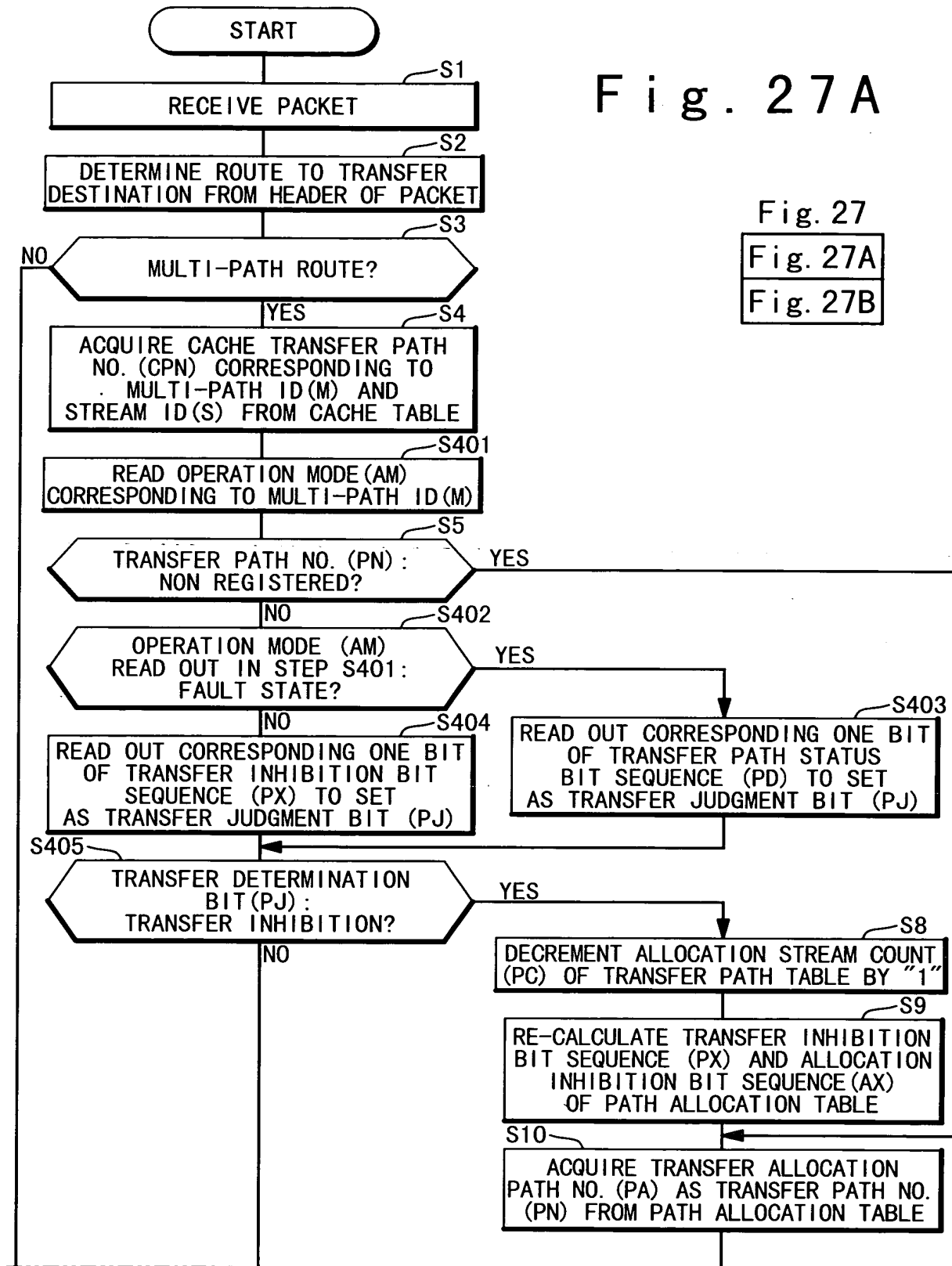
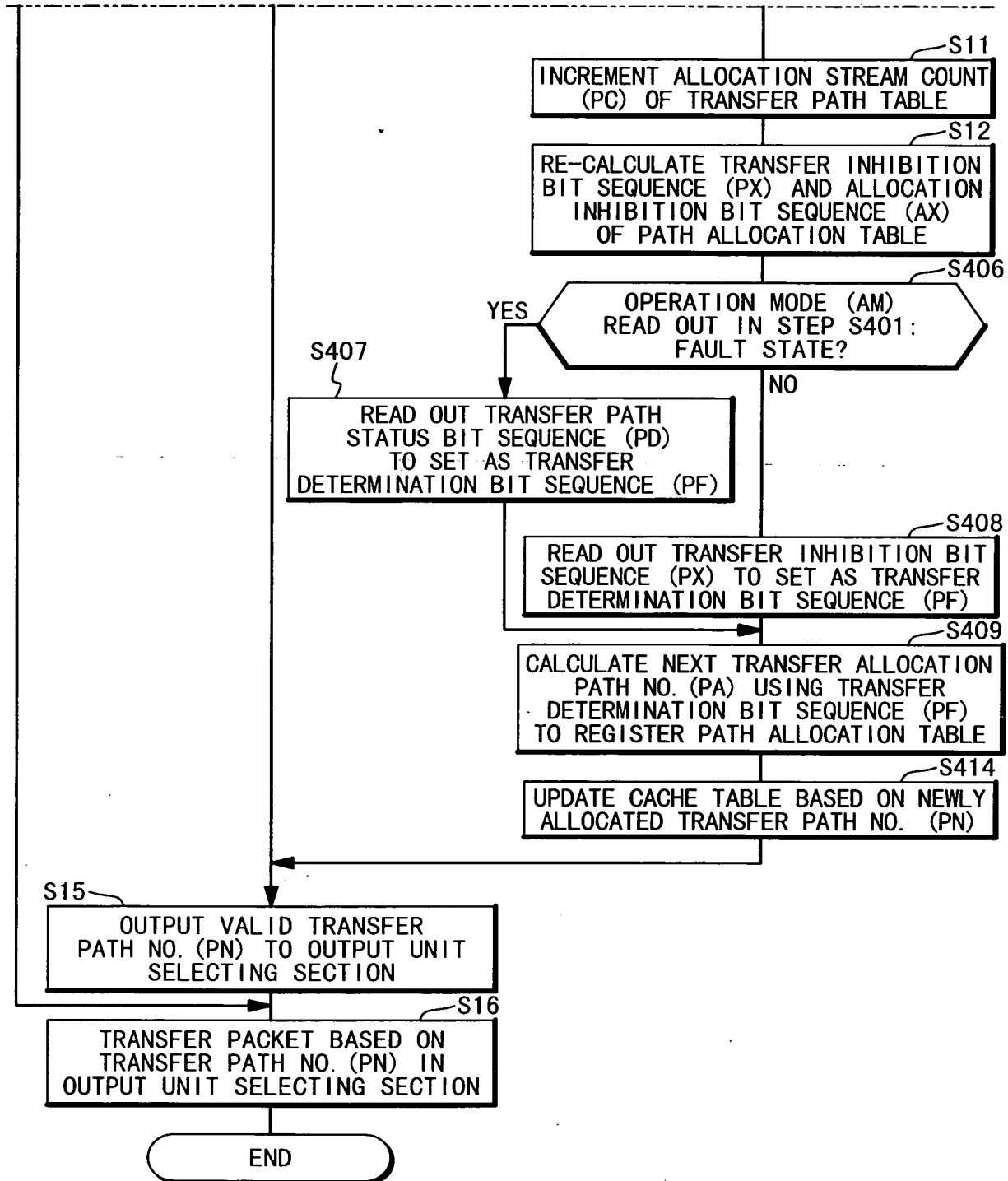


Fig. 27B



2000042260

Fig. 28

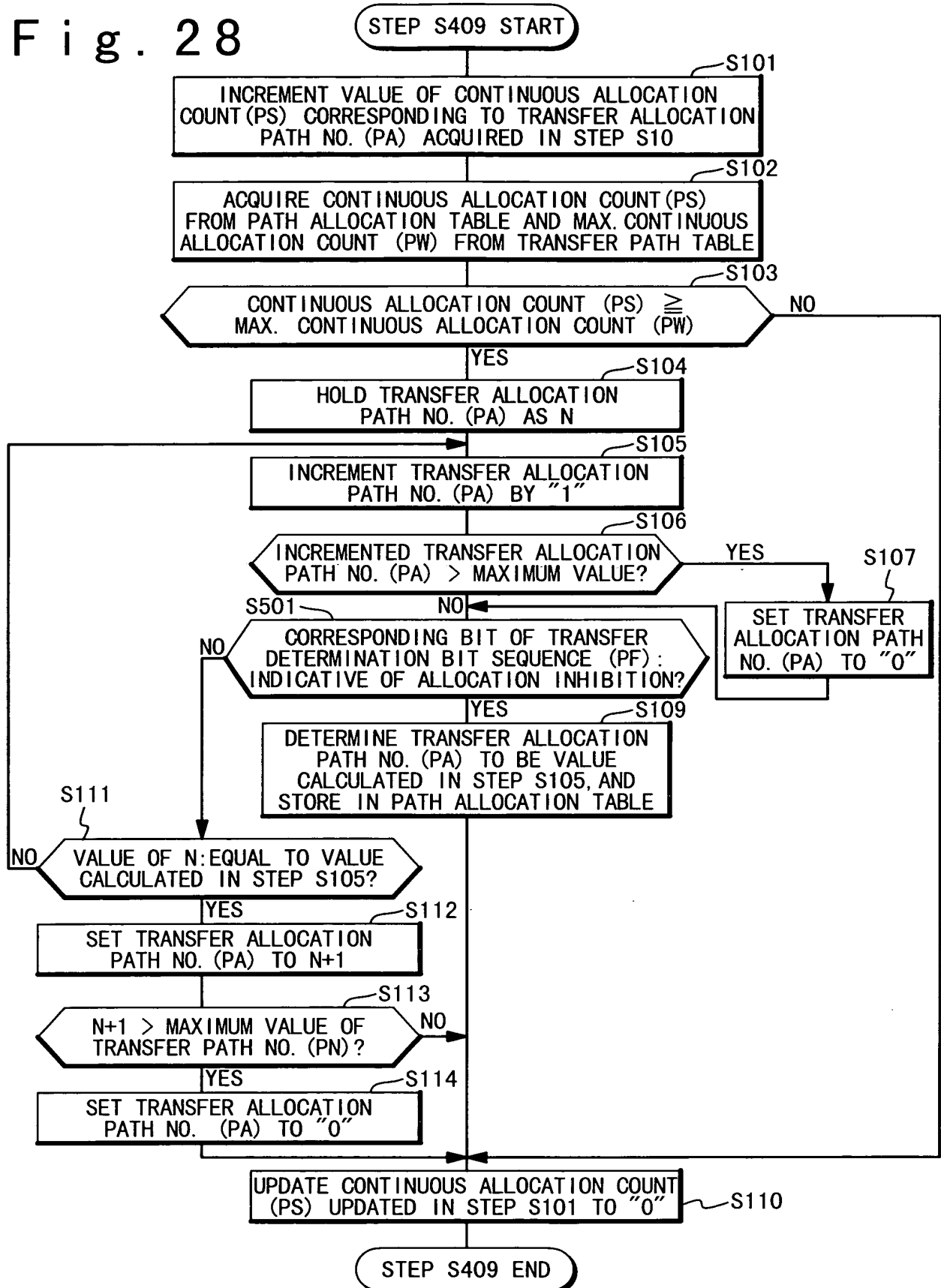


Fig. 29

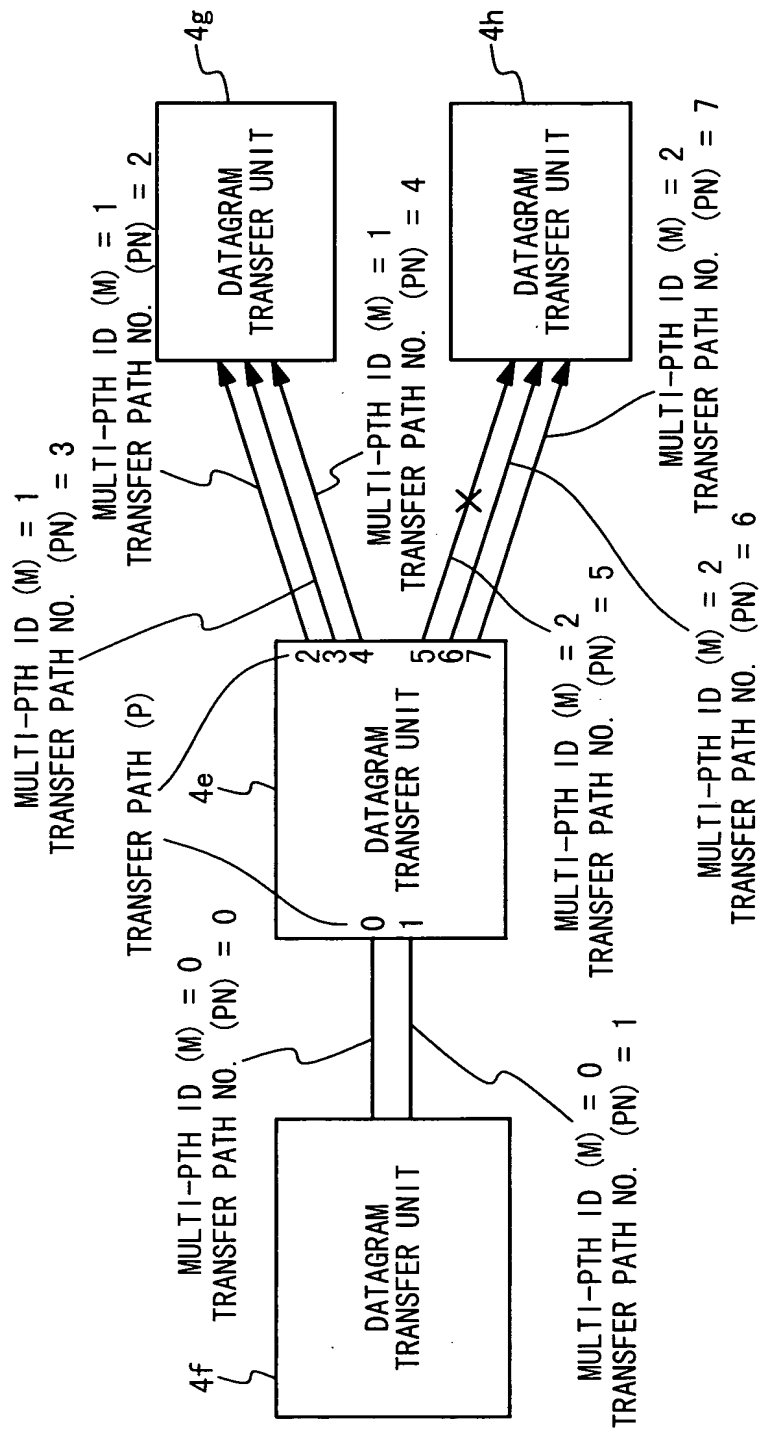


Fig. 30

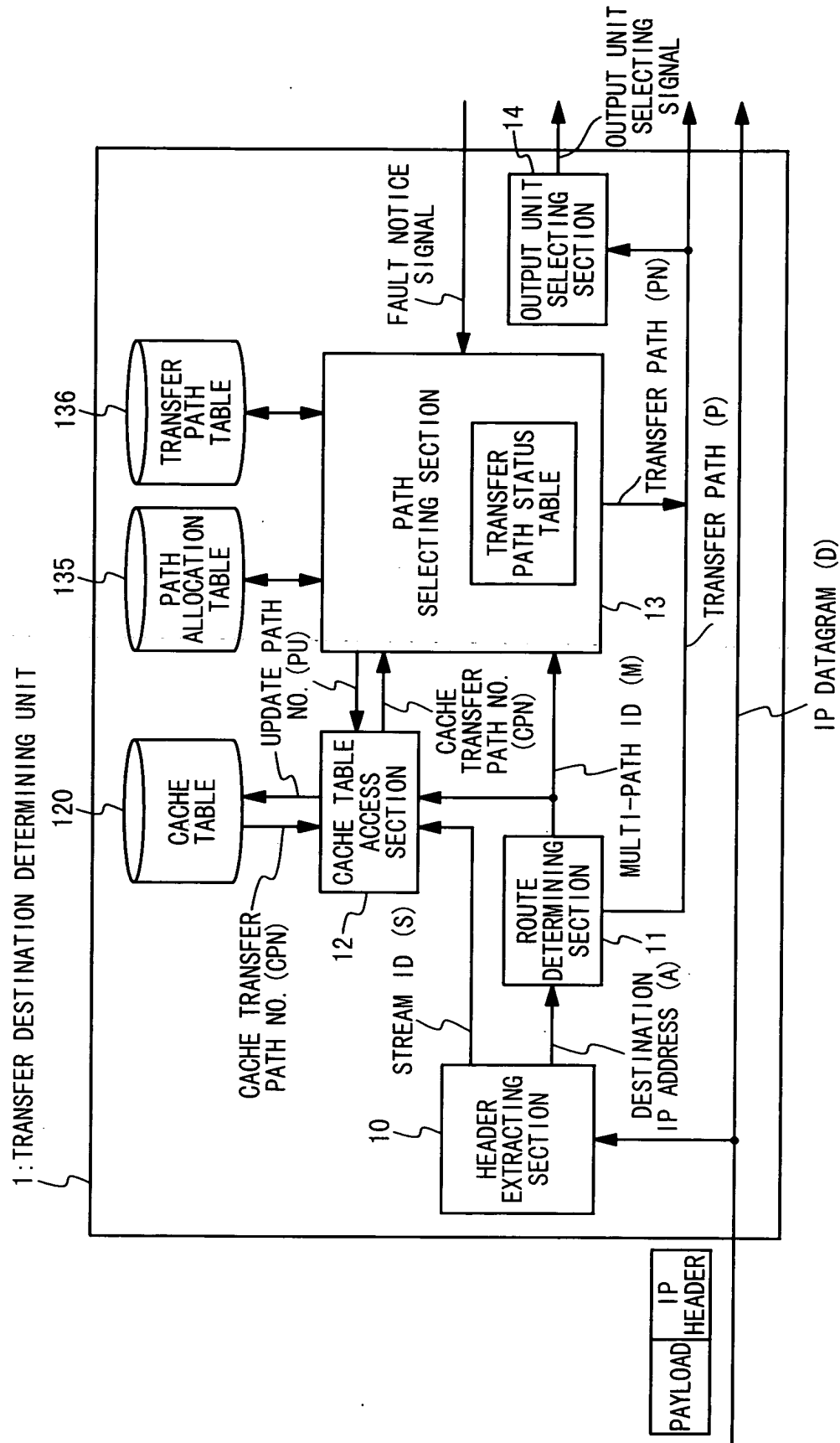


Fig. 31

135: PATH ALLOCATION TABLE

ADDRESS SECTION		DATA SECTION			
MULTI-PATH ID (M)	USE PATH BIT SEQUENCE (UP)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)
0	11111100	11111100	11111111	0	0
1	11100011	11100011	11111111	0	0
2	00011111	00011111	11111111	0	0

Fig. 32

136: TRANSFER PATH TABLE

ADDRESS SECTION		DATA SECTION		
MULTI-PATH ID (M)	TRANSFER PATH NO. (PN)	ALLOCATION STREAM COUNT (PC)	MAX. STREAM COUNT (PH)	MAX. CONTINUOUS ALLOCATION COUNT (PW)
0	0	2048	2048	1
	1	2048	2048	1
	2	0	0	0
	3	0	0	0
	4	0	0	0
	5	0	0	0
	6	0	0	0
	7	0	0	0
1	0	0	0	0
	1	0	0	0
	2	1365	1365	1
	3	1365	1365	1
	4	1366	1366	1
	5	0	0	0
	6	0	0	0
	7	0	0	0
2	0	0	0	0
	1	0	0	0
	2	0	0	0
	3	0	0	0
	4	0	0	0
	5	1365	1365	1
	6	1365	1365	1
	7	1366	1366	1

Fig. 33

137: TRANSFER PATH STATUS TABLE

TRANSFER PATH STATUS BIT SEQUENCE (PD)
00000000

Fig. 34

135: PATH ALLOCATION TABLE

ADDRESS SECTION		DATA SECTION				
MULTI-PATH ID (M)	USE PATH BIT SEQUENCE (UP)	TRANSFER INHIBITION BIT SEQUENCE (PX)	ALLOCATION INHIBITION BIT SEQUENCE (AX)	TRANSFER ALLOCATION PATH NO. (PA)	CONTINUOUS ALLOCATION COUNT (PS)	
0	11111100	11111100	11111111	0	0	
1	11100011	11100011	11111111	0	0	
2	00011111	00011111	11111111	0	0	

137: TRANSFER PATH STATUS TABLE

Fig. 35

TRANSFER PATH STATUS BIT SEQUENCE (PD)
00000000

Fig. 36

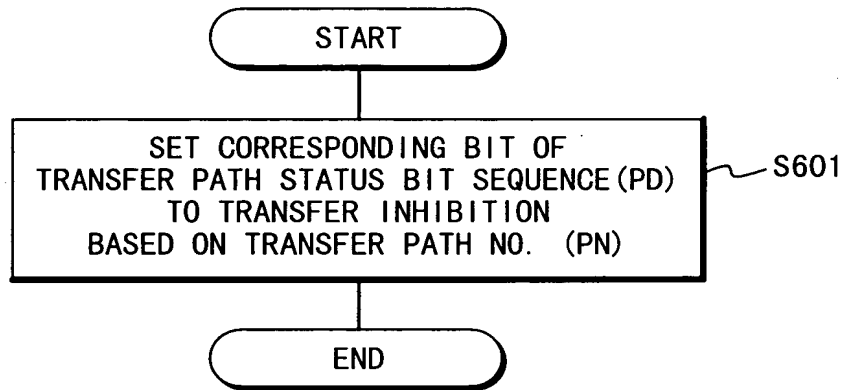


Fig. 37

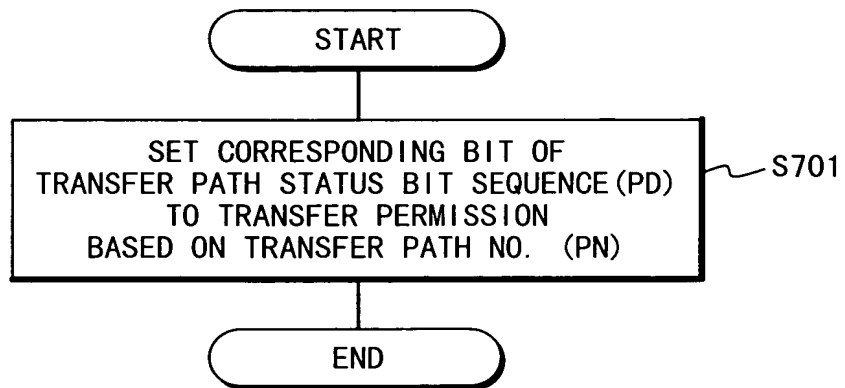


Fig. 38A

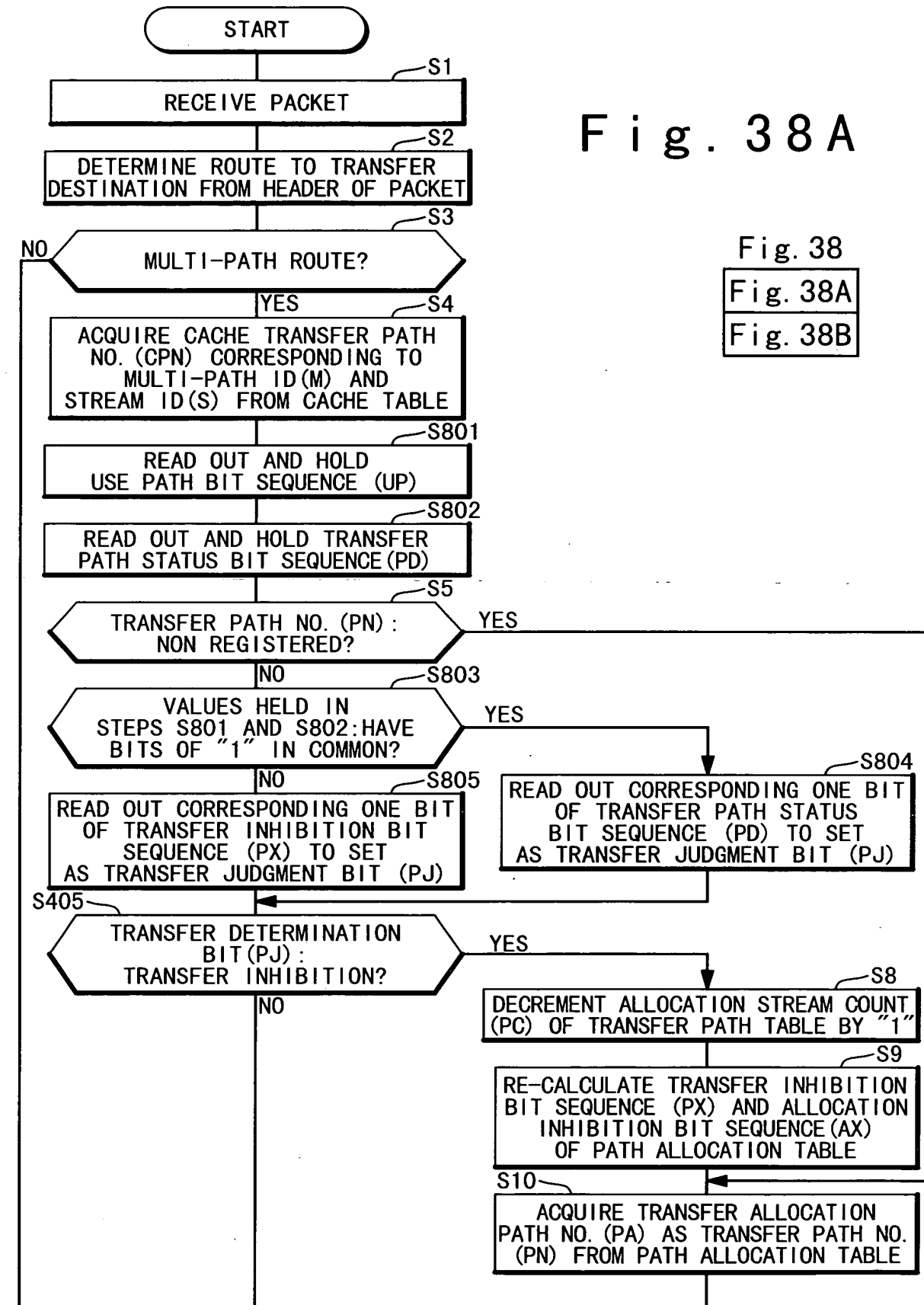


Fig. 38

Fig. 38A

Fig. 38B

Fig. 38A

Fig. 38B

